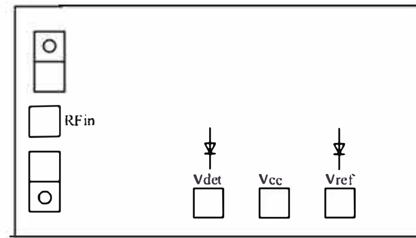
GPD-1860
GaAs MMIC Positive Peak Power Detector Chip

Performance characteristics

- Frequency range: 18GHz-60GHz
- Detection sensitivity: 220mV/mW
- Return loss: ≤ -9.5dB
- Dynamic range: 30dB
- Chip size: 1.25mm x 0.70mm x 0.07mm

Functional Block Diagram



Product Introduction

The positive peak power detector chip is made using GaAs Schottky diode technology, and the chip is grounded through a back through-hole. Operating frequency 18GHz-60GHz, powered by a +5V power supply. The Vdet single ended output detection voltage has a positive slope and can compensate for temperature deviation by subtracting it from the Vref voltage.

Microwave electrical parameters (TA=+25 ° C, Vcc=+SV, Pj : OdBm, Load open circuit)

Index	Symbol	Min	Typ	Max	Unit
Operating Frequency	f_{in}	18		60	GHz
Detection Sensitivity	β_V		220		mV/mW
Return Loss	RL			-9.5	dB
Detectlon Voltage Difference	V_{diff}	20		2000	mV
Dynamic Range	D_r		30		dB
Working Current	I_{CC}		0.9		mA

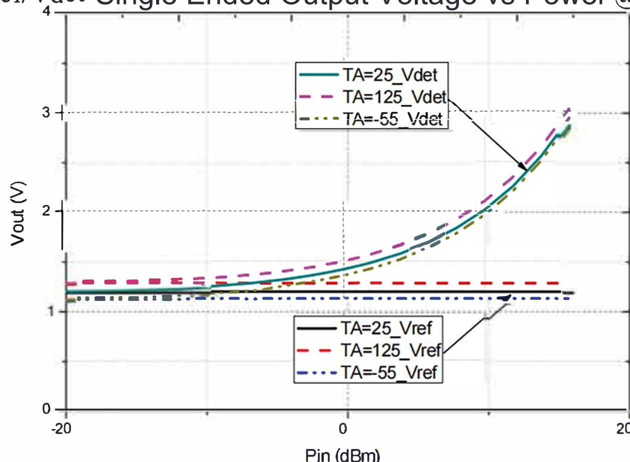
The formula for calculating the detection voltage difference is $V_{diff}=|V_{det}-V_{ref}|$, V_{det} is the detection output voltage, and Vrcf is the reference output voltage of about 1.2V.

Use Restriction Parametersrs

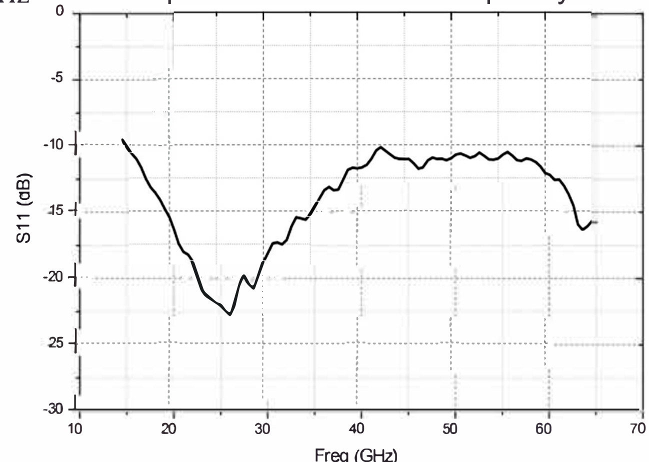
Parameter	Symbol	Limit Value
Maximum Input Power	P_p	+20dBm
Maximum Operating Voltage	V_{max}	6V
OperatingTemperature	T_{op}	-55℃～+125℃
Storage Temperature	T_{STG}	-65℃～+150℃

Typical curve (Test conditions: T_A = +25℃, V_{CC}=5.0V, P_i: 0dBm, Load open circuit)

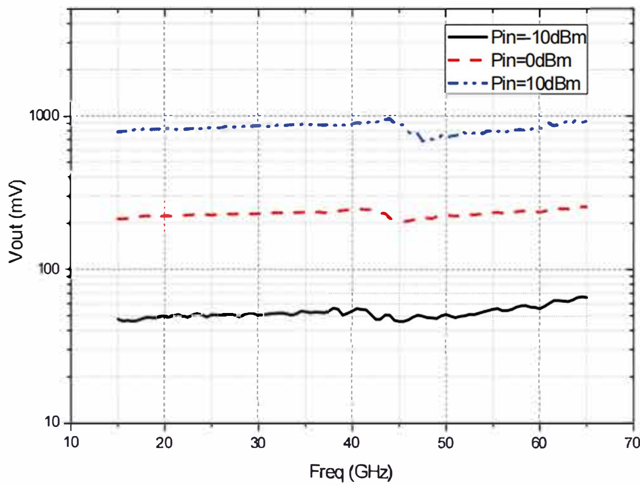
Vref/Vdet Single Ended Output Voltage vs Power @20GHz



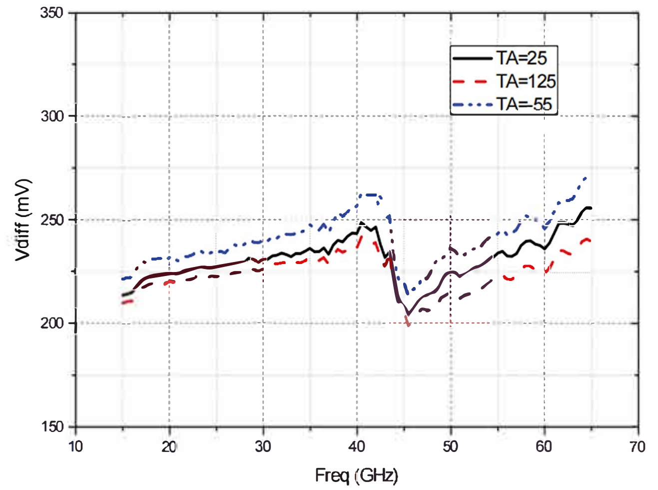
Input Return Loss vs. Frequency



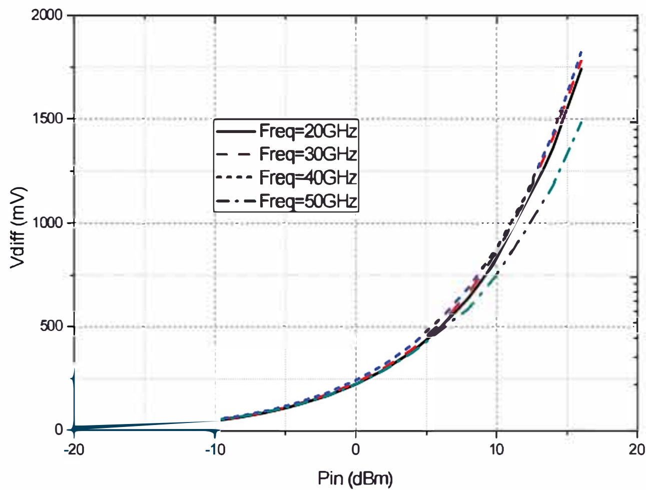
Detecting Voltage Dfference $|V_{diff}|$ vs. Fquency



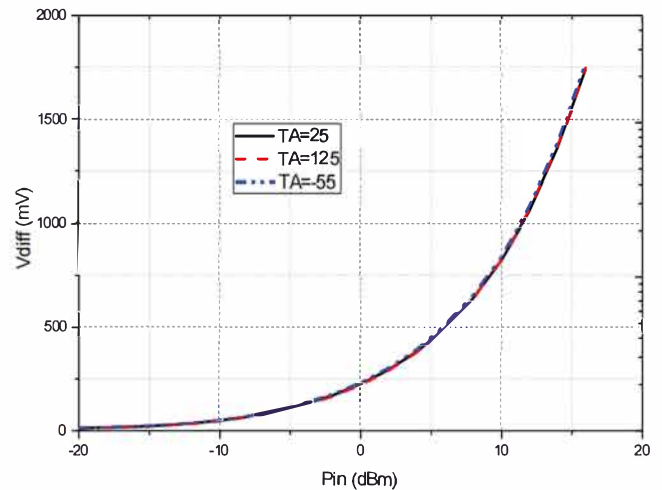
Detection Sensitivity vs Frequency



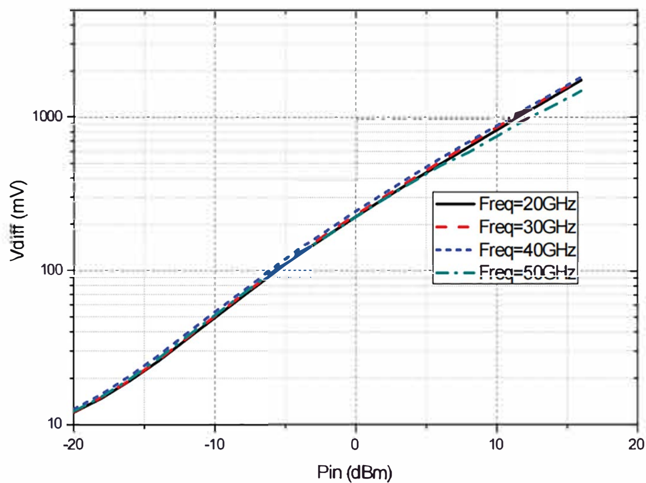
Detecting Voltage Dfference $|V_{diff}|$ vs Power



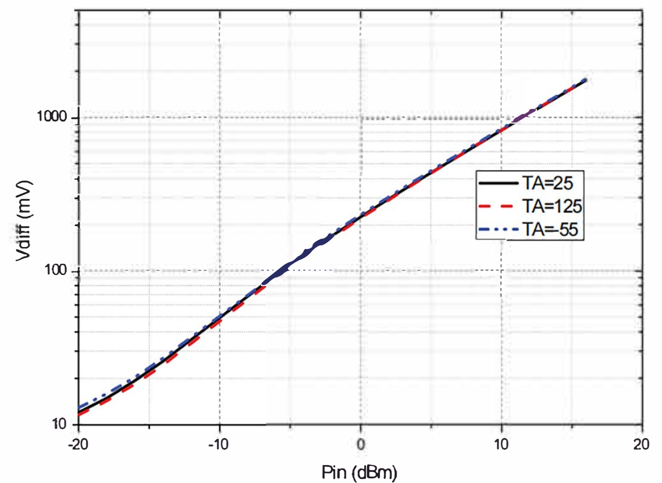
Detecting Voltage Dfference $|V_{diff}|$ vs Power@20GHz



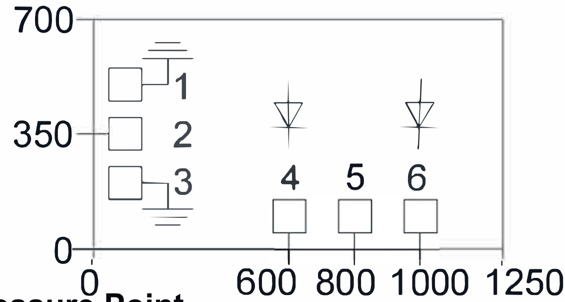
Detecting Voltage Dfference $|V_{diff}|$(LOG) vs. Power



Detecting Voltage Dfference $|V_{diff}|$(LOG) vs. Power@20GHz



Outline Dimensions and Pressure Point Arrangement Diagram



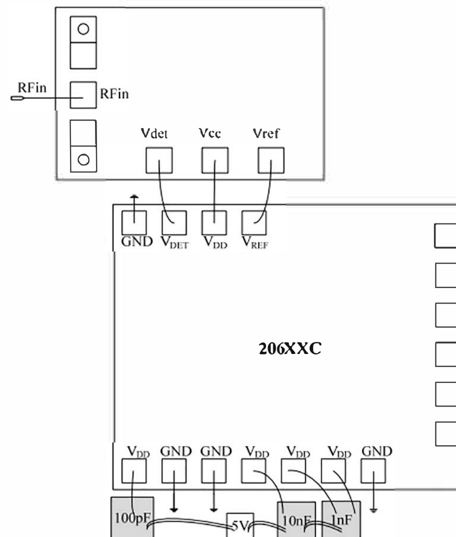
Note: The units in the figure are all micrometers (μm); The tolerance of the external dimensions is ± 100 μm.

Definition of Bonding Pressure Point

Pressure Point No.	Function Symbol	Function Description	PAD Dimensions
1	GND	Grounding point (for probe testing only)	$100\times100\mu m^2$
2	RFin	RF signal input terminal	$100\times100\mu m^2$
3	GND	Grounding point (for probe testing only)	$100\times100\mu m^2$
4	Vdet	Detection voltage output terminal	$100\times100\mu m^2$
5	Vcc	Power supply terminal	$100\times100\mu m^2$
6	Vref	Reference voltage output terminal	$100\times100\mu m^2$

Typical applications

The positive peak power detector is matched with the differential amplifier driver series products, which can perform detection voltage differential amplification operation, achieve temperature compensation function, improve detection sensitivity, enhance driving capability and accelerate response speed. It is mainly used for power judgment, power indication, gain control, signal demodulation, load condition and frequency range analysis and other functions.

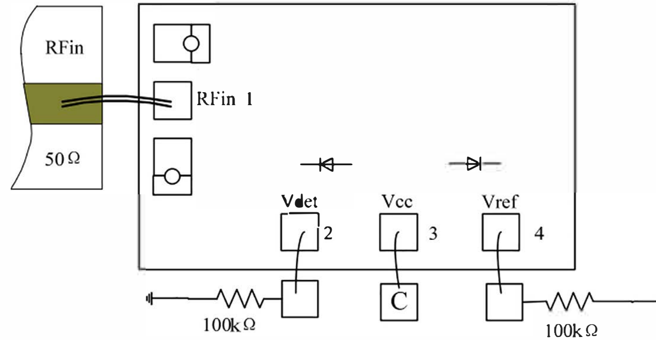


Application Description:

1) The RF end of Rfin needs to add isolation capacitors according to usage conditions, and different chip power ends need to add filtering capacitors as required;
2) During typical curve testing, Rfin-PAD does not have bonding wires. It is recommended to use two microwave signal bonding wires with a length of less than 300 μm.
3) When using various instruments such as oscilloscopes to test electrical characteristics, it is necessary to consider the equivalent load conditions of the probe and testing instrument to prevent testing errors caused by inappropriate loads, which can easily lead to device damage. It is recommended to use the high-speed probe (load capacity ≤ 12pF) that comes with the oscilloscope and other instruments or add a resistance greater than 1k ohms at the testing end for protection.
4) For the cascading use of detectors and NC206XXC series differential amplifier drivers, please refer to the "Product Manual for Detection Specific Differential Amplifier Drivers".

Suggested Assembly Diagram

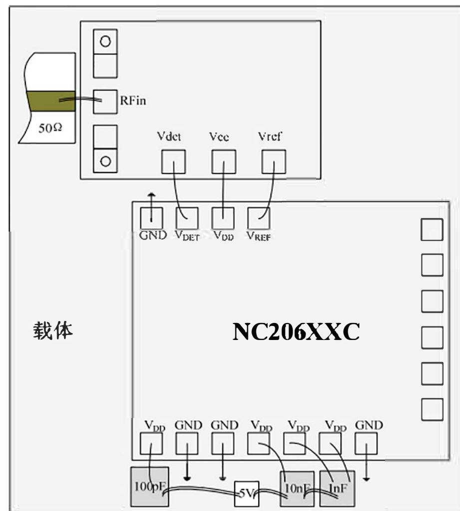
1. Single use



Note:

1. Vee requires an additional chip filtering capacitor of 1000pF at the power supply end;
2. The external equivalent resistance of Vdet and Vref terminals should be greater than 100k ohms;
3. RFin-PAD without bonding wire during typical curve testing;
4. The distance between the microwave signal connection line and the chip should be within 100 μm.

2. Cascade use



Note:

1) Assembly and use in purifying environments;
2) GaAs material is very brittle and the chip surface is easily damaged (do not touch the surface), so caution must be taken when using it;
3) Use 1-2 bonding wires (25 μ m diameter gold wire) for input and output, and keep the bonding wires as short as possible, not larger than 300 μ m; The back of the chip must be grounded;
4) Use 80/20 gold tin sintering, with a sintering temperature not exceeding 300'C and a sintering time as short as possible, not exceeding 30 seconds; This product is a sensitive electrostatic device. Please pay attention to anti-static measures during storage and use;
5) Dry and nitrogen storage environment;
6) Do not attempt to clean the surface of the chip using dry or wet chemical methods;
7) Please contact the supplier if you have any questions.

This product is sensitive to static electricity, please pay attention to anti-static measures during use