

Performance Characteristics

- ✧ Output Frequency: 30GHz-53GHz
- ✧ Output Power: -2dBm@Pin= 15dBm
- ✧ Conversion Loss: 17dB
- ✧ f_0 、 $2f_0$ Suppression: 20dBc
- ✧ Chip Size: 1.04 mmx0.86 mmx0.07 mm

Product Introduction

The Q-band triple frequency converter chip covers a frequency range of 30GHz-53GHz. When the input power is 15dBm, the typical value of in band output power is -2dBm, the typical value of frequency conversion loss is 17dB, and the typical values of fundamental and second harmonic suppression are 20dBc

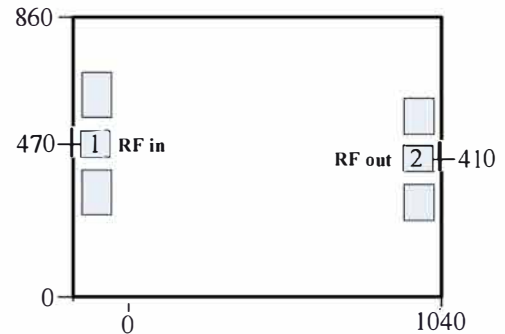
Electrical Parameters (T_A=+25°C)

Parameters	Min	Typ	Max	Unit
Input Frequency	10		17.7	GHz
Output Frequency	30		53	GHz
Input Power		15		dBm
Output Power		-2		dBm
Conversion Loss		17		dB
f_0 、 $2f_0$ suppression		20		dBc

Use Restriction Parameters

Input Power	20dBm
Storage Temperature	-65°C~150°C
Operating Temperature	-55°C~85°C

External Dimensions

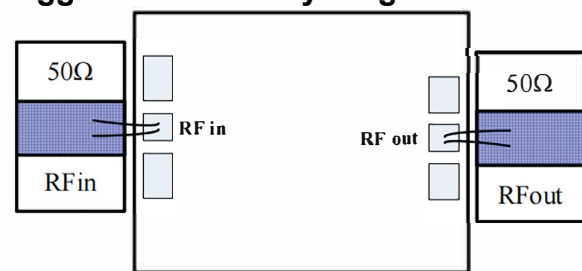


- Note: 1) All dimensions marked are in micrometers (μm):
 2) Dimensional tolerance for external dimensions: $\pm 50 \mu\text{m}$;
 3) The chip thickness is $70 \mu\text{m}$.

Definition of Bonding Pressure Point

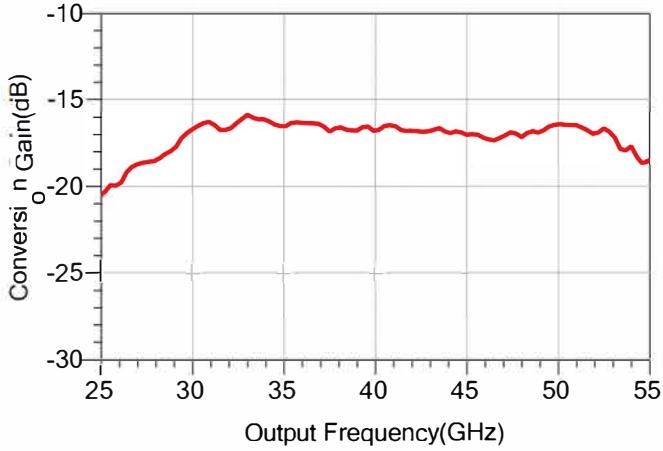
No.	Symbol	Function	Dimensions (μm^2)
1	RF in	RF signal input terminal, external 50 ohm system, no need for DC isolation capacitor	70×70
2	RFout	RF signal output terminal, external 50 ohm system, no need for DC isolation capacitor	70×70

Suggested Assembly Diagram

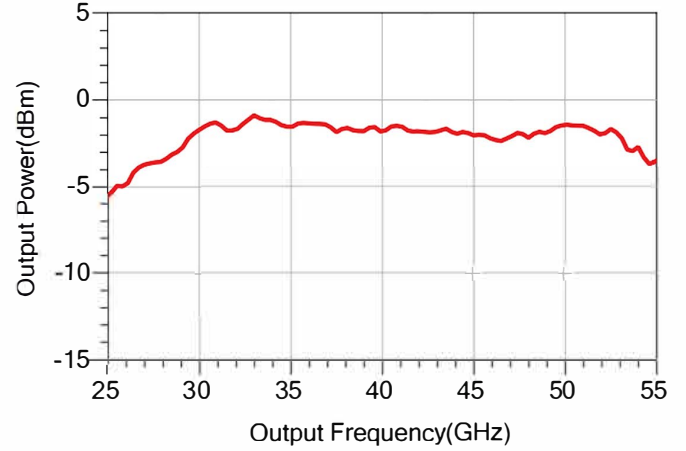


On Chip Testing Curve (T_A=+25°C)

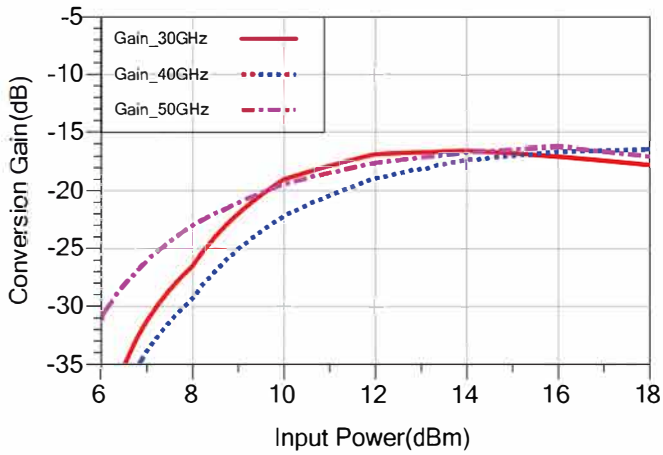
Conversion Loss vs. Output Frequency @ Pin=15dBm



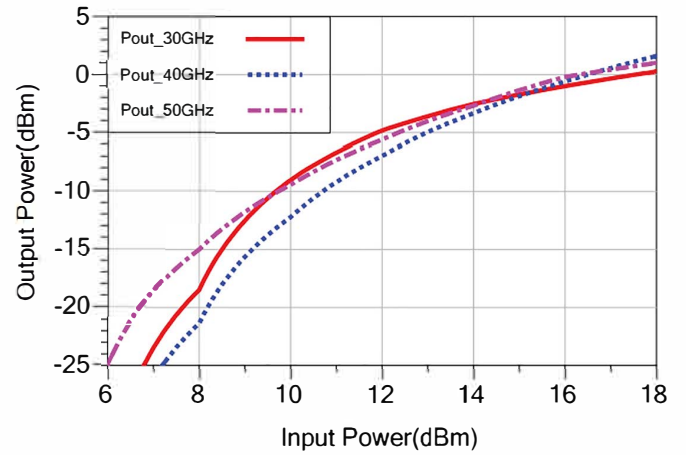
Output Power vs Output Frequency @ Pin=15dBm



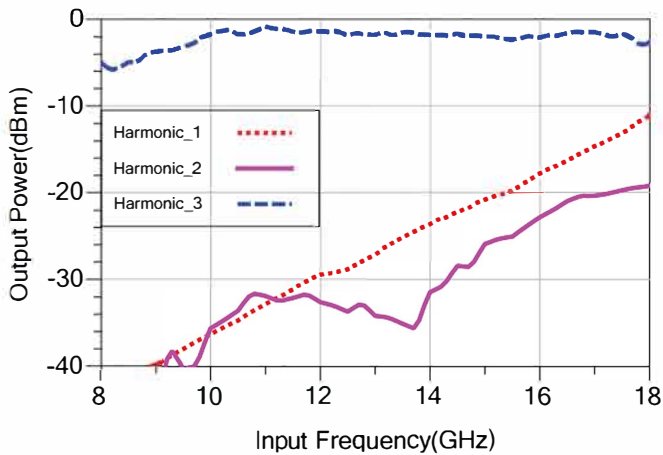
Conversion Loss vs Input Power



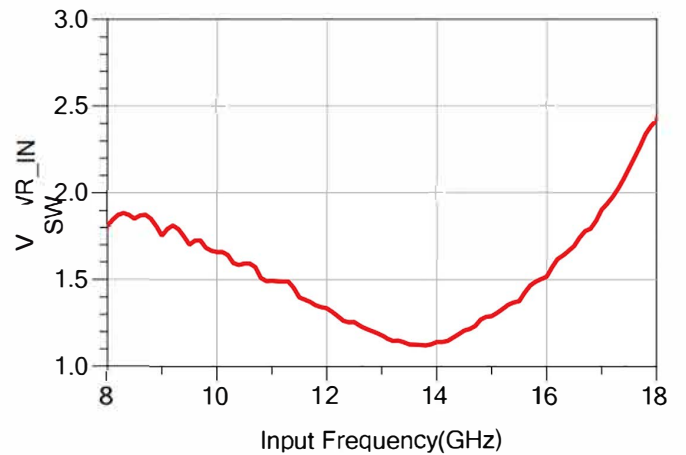
Output Power vs Input Power



Harmonic Output Power vs Input Frequency @ Pin=15dBm



Input Standing Wave vs Input Frequency @ Pin=15dBm



Note:

- 1) Storage: The chip must be placed in a container with electrostatic protection and stored in a nitrogen environment.
 - 2) Cleaning treatment: Bare chips must be operated and used in a purified environment, and it is prohibited to use liquid cleaning agents to clean the chips.
 - 3) Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.
 - 4) Conventional operation: To retrieve the chip, please use a vacuum chuck or a precision pointed tip. During the operation, avoid touching the chip surface with tools or fingers.
 - 5) When powering on in sequence, apply gate voltage first and then drain voltage; When turning off the power, first remove the leakage voltage, and then remove the shed voltage.
 - 6) Mounting operation: Chip installation can be carried out using AuSn solder eutectic sintering or conductive adhesive bonding process. The mounting surface must be clean and flat, and the gap between the chip and the input/output RF connection substrate should be minimized as much as possible.
Sintering process: Use 80/20AuSn for sintering, with a sintering temperature not exceeding 300 °C, a sintering time as short as possible, not exceeding 20 seconds, and a friction time not exceeding 3 seconds.
Adhesive process: When bonding conductive adhesive, try to minimize the amount of glue applied, and refer to the information provided by the conductive adhesive manufacturer for curing conditions.
 - 7) Bonding operation:
Unless otherwise specified, use 2 bonding wires (25 μm diameter gold wire) for RF input and output, and keep the bonding wires as short as possible.
Hot ultrasonic bonding temperature is 150 °C, using as little ultrasonic energy as possible.
 - 8) Please contact the supplier if you have any questions.
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